HD-Sec: Holistic Design of Secure Systems on Capability Hardware

DSbD
Digital Security by Design

https://hd-sec.github.io

Colin Snook, Asieh Salehi, Thai Son Hoang, Robert Thorburn, Michael Butler, Leonardo Aniello, Vladimiro Sassone
University of Southampton, UK {cfs, a.salehi-fathabadi, , t.s.hoang, robert.thorburn , m.j.butler, l.aniello, vsassone}@soton.ac.uk

University of Southampton
UKRI Engineering and Physical Sciences Research Council

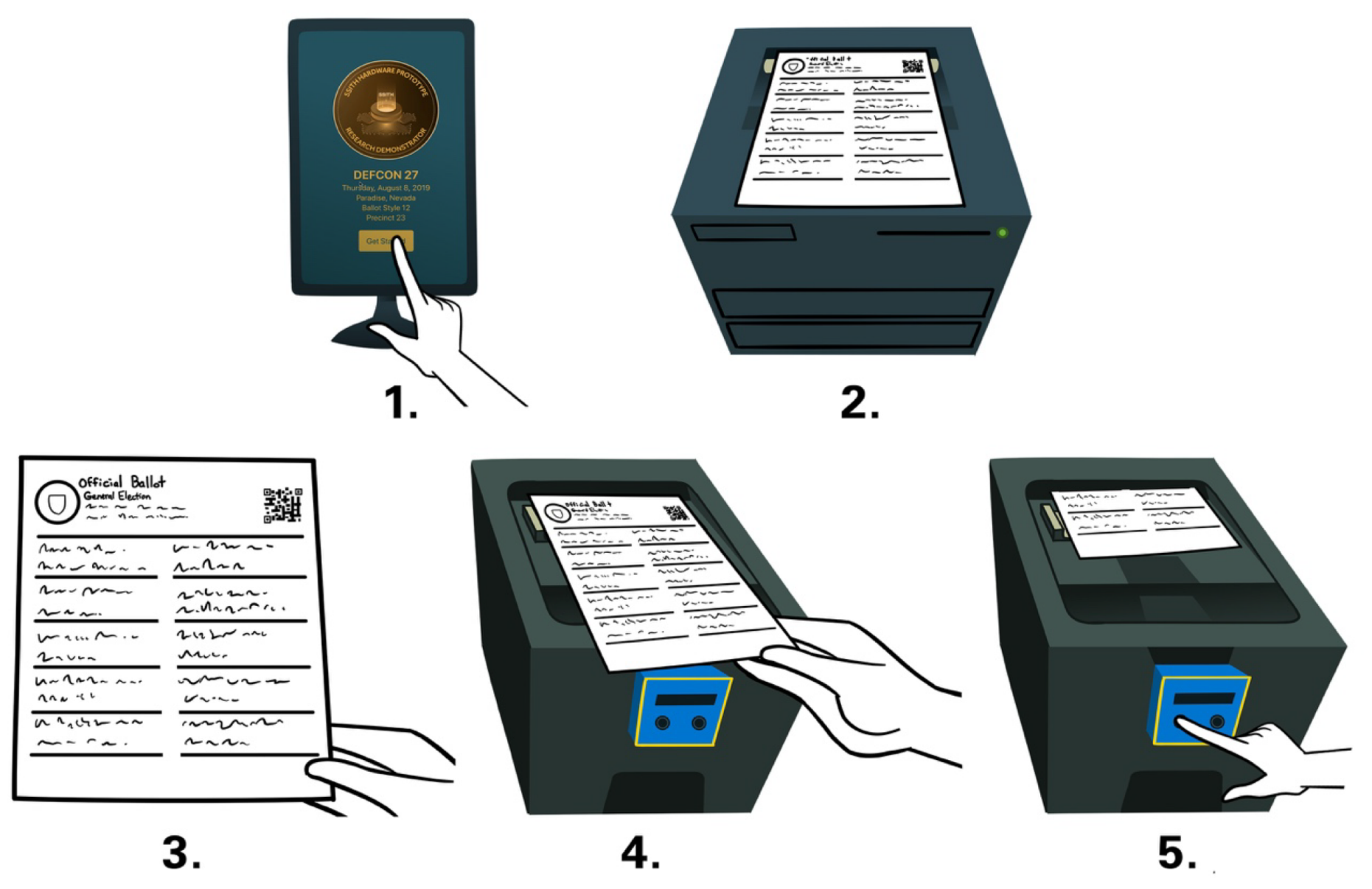
Project Overview

Transformation of security-critical software development

- From an expensive iterative test-and-fix approach
  - To a correctness-by-construction (CxC) approach
- The design of software from requirements to implementation
  - Formal modelling, Reusable formal abstractions
  - Verification
  - Model transformation
  - CxC tools and running on capability hardware

Case Study: Smart Ballot Box[1] (SBB)

- **Availability:** the voter should not be prevented from casting a ballot.
- **Confidentiality :** the voter's choices should be secret
- **Integrity:** the system should only accept valid ballots and reject invalid ballots.



Designing Error handling for CHERI exceptions

- Error handling allows runtime management of hardware-detected memory attacks, security solutions can be designed into the system.
- Exception handling needs to be context and application specific:
  - UML-B modelling to develop application-specific error handling behaviour for critical component

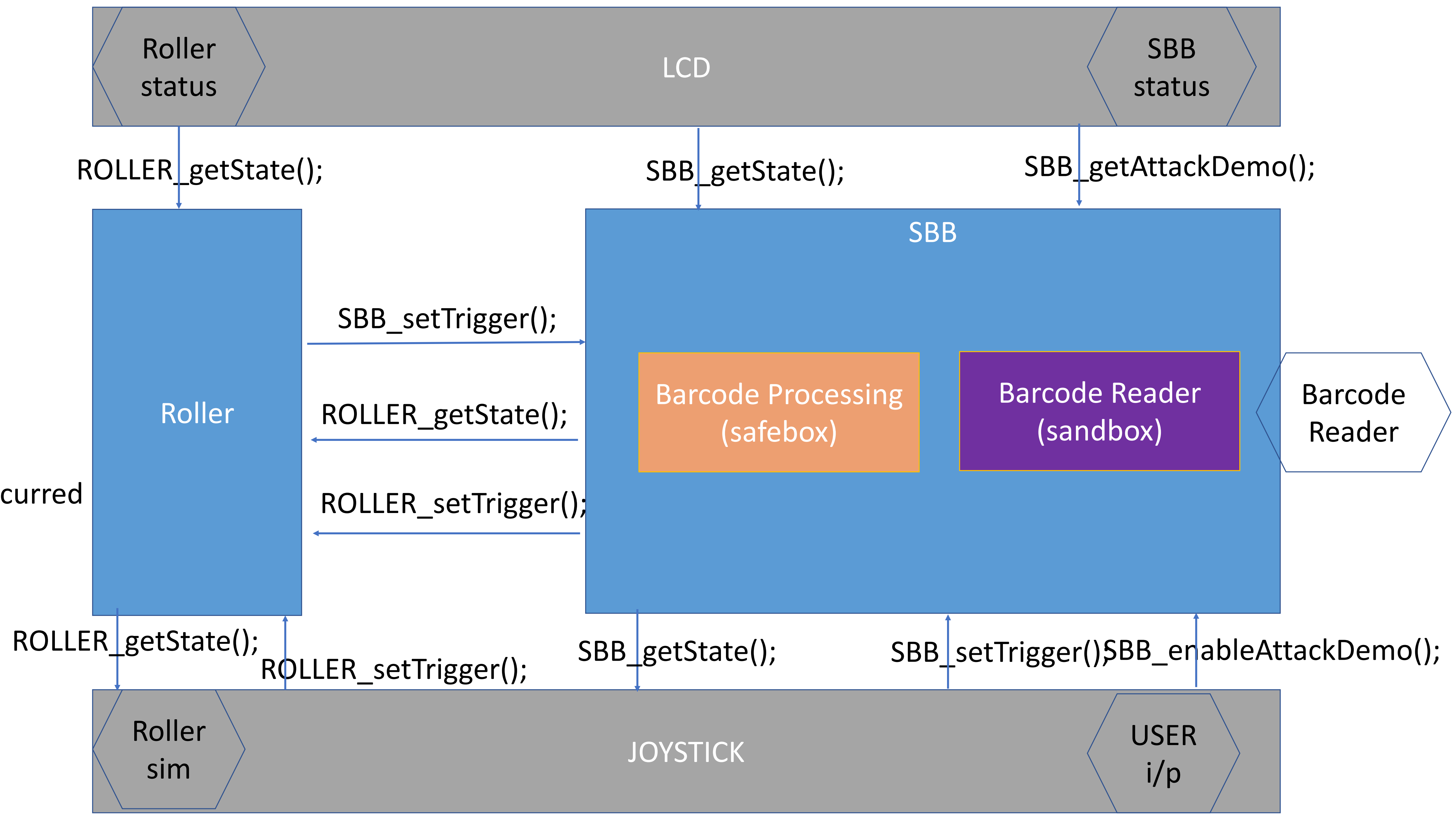
SBB Sonata - Compartment structure

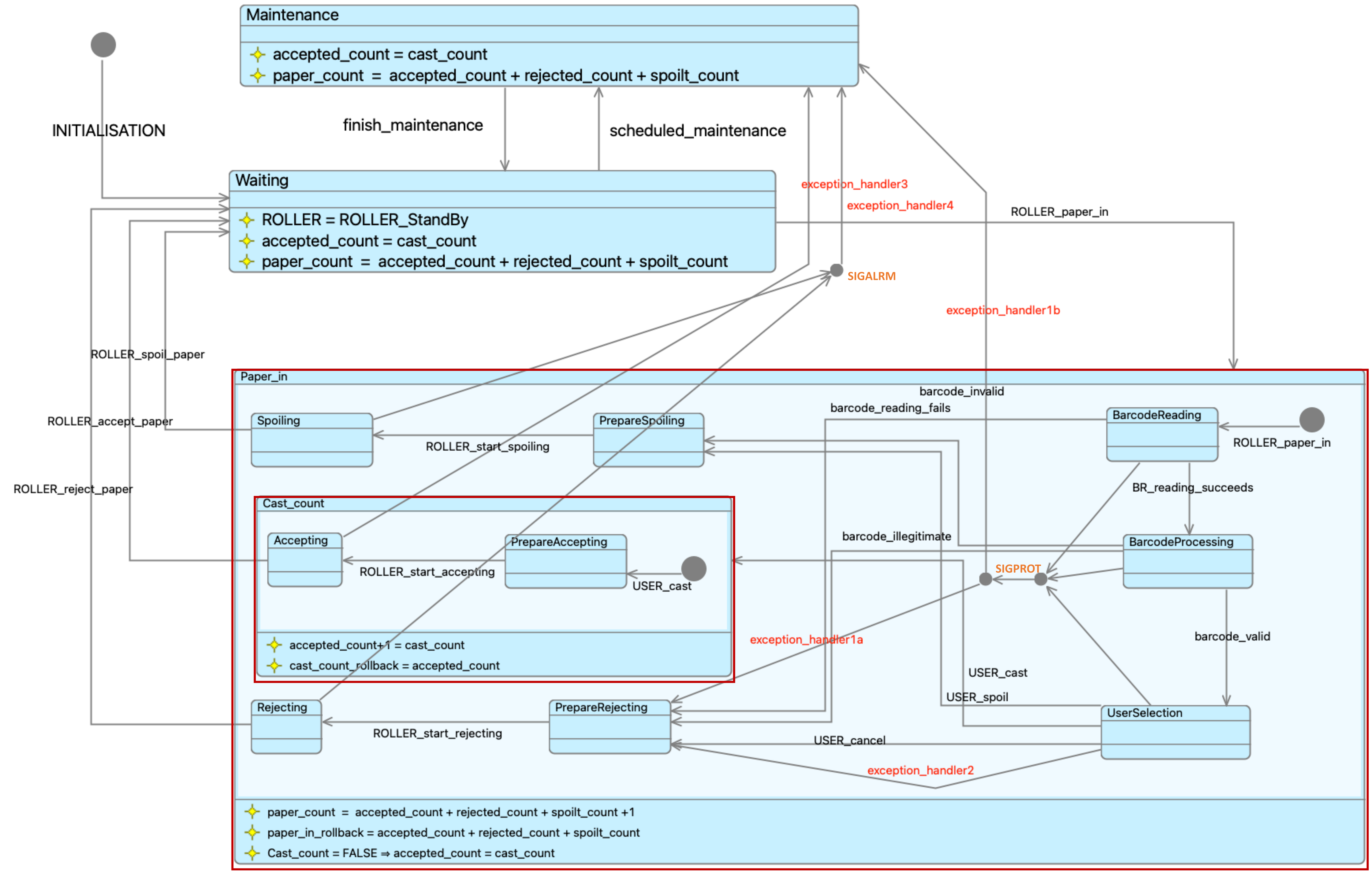
- CHERI compartments provide support for
- structuring/containment of error-handling
- data encapsulation
- Two Top level Thread compartments
- Roller and SBB
- Two Library compartments
- Barcode Reader and Barcode Processing

SBB formal model - Implementation for Sonata board

- State encoding of implementation enables rich error handling
- Error handler uses state to determine where the exception occurred
- Error handler uses state to initiate a recovery state

- Statemachines implemented as *switch (state)*
- Transitions implemented as *functions*
- Exception transitions are implemented In the Cheri *compartment_error_handler*





References

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